SYSTEM FOR ADJUSTING A POWER SUPPLY LEVEL OF A DIGITAL PROCESSING COMPONENT AND METHOD OF OPERATING THE SAME

ABSTRACT OF THE DISCLOSURE

There is disclosed control circuitry for adjusting a power supply level, VDD, of a digital processing component having varying operating frequencies. The control circuitry comprises N delay cells and power supply adjustment circuitry. The N delay cells are coupled in series, each of which has a delay D determined by a value of VDD, such that a clock edge applied to an input of a first delay cell ripples sequentially through the N delay cells. The power supply adjustment circuitry capable of adjusting VDD and is operable to (i) monitor outputs of at least a K delay cell and a K+1 delay cell, (ii) determine that the clock edge has reached an output of the K delay cell and has not reached an output of the K+1 delay cell, and (iii) generate a control signal capable of adjusting VDD in response thereto.